CLAIMS:

What is claimed is:

1. A method in a data processing system for testing hardware in a data processing system having multiple partitions, the method comprising:

initializing a monitor process in a first partition assigned to a first processor; and

initializing a random code generation process in a second partition associated with a second processor, wherein the random code generation process generates instructions and executes the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.

2. The method of claim 1, wherein the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed.

3. The method of claim 2, wherein the random code generation process calls a function to store data for the heartbeat in a data structure.

4. The method of claim 3, wherein the monitor process monitors the random code generation process by checking the data structure.

5. The method of claim 1, wherein the first processor and the second processor are located in a single chip.

6. The method of claim 1 further comprising:

responsive to detecting an error executing the instructions in the second partition, preventing termination of the second partition.

7. A data processing system comprising:

a bus system;

a communications unit connected to the bus system;

a memory connected to the bus system, wherein the memory includes a set of instructions; and

a processing unit connected to the bus system, wherein the processing unit executes the set of instructions to initialize a monitor process in a first partition assigned to a first processor and initialize a random code generation process in a second partition associated with a second processor in which the random code generation process generates instructions and executes the instructions to test the second processor and in which the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.

8. A data processing system for testing hardware in a data processing system has multiple partitions, the data processing system comprising:

first initializing means for initializing a monitor process in a first partition assigned to a first processor; and

second initializing means for initializing a random code generation process in a second partition associated with a second processor, wherein the random code generation process generates instructions and executes

the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.

9. The data processing system of claim 8, wherein the random code generation process generates a heartbeat used by the monitor process to determine whether the random code generation process has failed.

10. The data processing system of claim 9, wherein the random code generation process calls a function to store data for the heartbeat in a data structure.

11. The data processing system of claim 10, wherein the monitor process monitors the random code generation process by checking the data structure.

12. The data processing system of claim 8, wherein the first processor and the second processor are located in a single chip.

13. The data processing system of claim 8 further comprising:

preventing means, responsive to detecting an error executing the instructions in the second partition, for preventing termination of the second partition.

14. A computer program product in a computer readable medium for testing hardware in a data processing system having multiple partitions, the computer program product comprising:

first instructions for initializing a monitor process in a first partition assigned to a first processor; and

second instructions for initializing a random code generation process in a second partition associated with a second processor, wherein the random code generation process generates instructions and executes the instructions to test the second processor and wherein the monitor process monitors the random code generation process and resets the second processors if the random code generation process fails.